REMARKS

This application has been carefully reviewed in light of the Office Action dated September 20, 2005. Claims 1 to 15 are now pending in the application, with Claims 11 to 15 having been newly-added. Claims 1, 6 and 11 are the independent claims herein. Reconsideration and further examination are respectfully requested.

The abstract was objected to for an informality that has been attended to by amendment as recited above. Withdrawal of the objection to the abstract is respectfully requested.

Claim 1 was objected to for informalities that have also been attended to by amendment as recited above. Withdrawal of the objection to Claim 1 is respectfully requested.

Claims 1 to 10 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,661,373 (Nishizawa). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention relates to controlling the release of a data signal line of a serial communication apparatus when sending and receiving serial data. According to the invention, a controller controls a buffer to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level. For example, when a mode to send a signal is switched to a mode to receive a signal, a control signal for instructing the release of the data signal line is input. In the present invention, the buffer is controlled to release the data signal line after the data signal line is temporarily retained at the second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at the first level. By the virtue of the foregoing,

since the data signal line is released after the data signal line has been temporarily retained at the second level, a blunt waveform of a signal can be prevented.

Referring specifically to the claims, Claim 1 is a serial communication apparatus for sending and receiving serial data through a data signal line, comprising buffer means capable of releasing the data signal line, and control means for controlling said buffer means to release the data signal line after the data signal line is temporarily retained at a second level if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level.

Claim 6 is a method claim that substantially corresponds to Claim 1, and Claim 11 is an apparatus claim (in non-means-plus-function form) that substantially corresponds to Claim 1.

The applied art is not seen to disclose or to suggest the features of independent Claims 1, 6 and 11, and in particular, is not seen to disclose or to suggest at least the feature of controlling a buffer to release a data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level.

Nishizawa is merely seen to disclose a method for transmitting binary digital signals in which a signal line is used for one way communication. Thus, as one difference between Nishizawa and the present invention, Nishizawa fails to disclose a serial communication apparatus for sending and receiving serial data through only one data signal line. In addition, Nishizawa discloses that binary digital signals are transmitted by using two kinds of pulses; one of which has a sharp waveform at the leading edge and a blunt sharp waveform at the trailing edge of the pulse, and the other of which has a blunt waveform at the leading edge and a sharp waveform at the trailing edge of the pulse. In

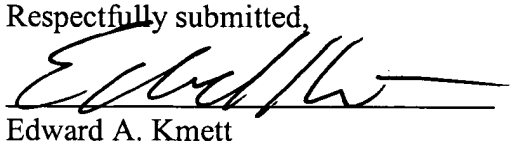
Nishizawa, it is disclosed that a three-state buffer is used for generating those kinds of pulses. However, Nishizawa fails to disclose or to suggest that the buffer is controlled to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level.

In view of the foregoing deficiencies of Nishizawa, Claims 1 to 15 are not believed to be anticipated. Accordingly, Claims 1 to 15 are believed to be allowable.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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